6523132

09/657482

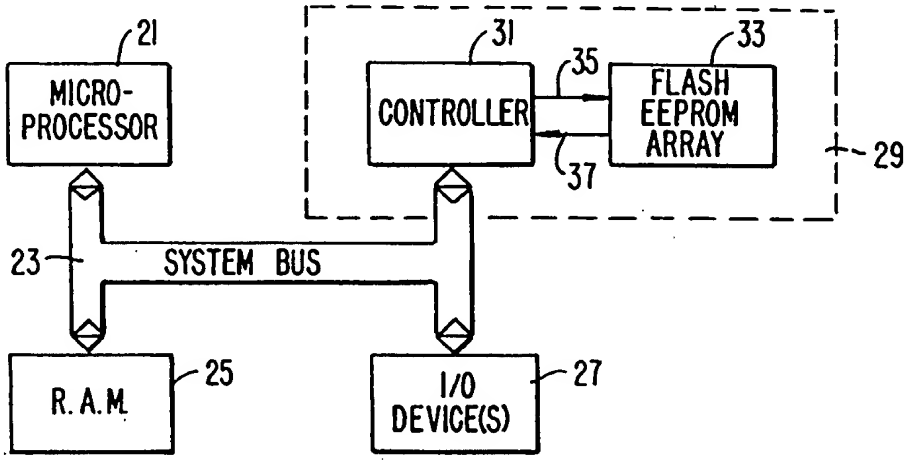

FIG._1A

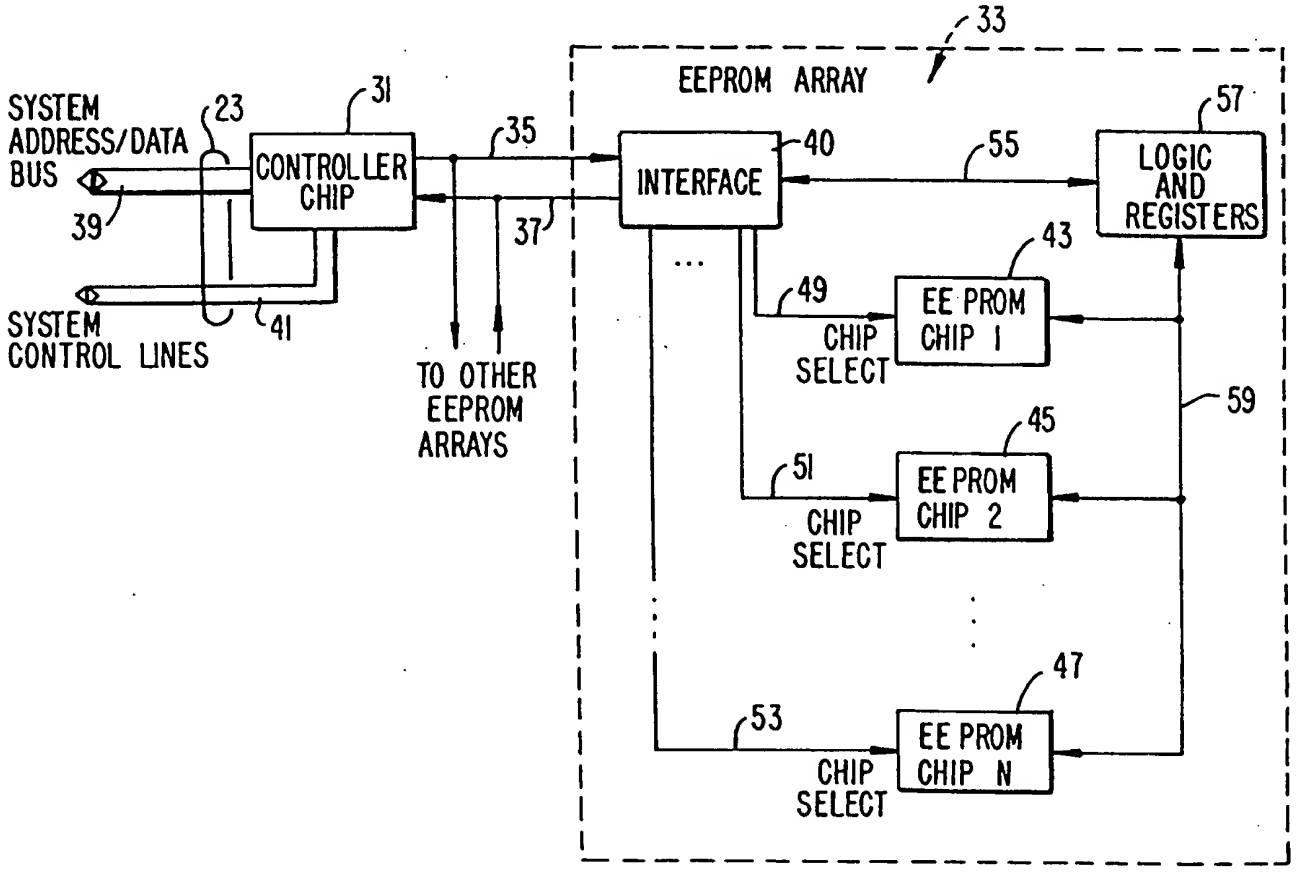

FIG._1B

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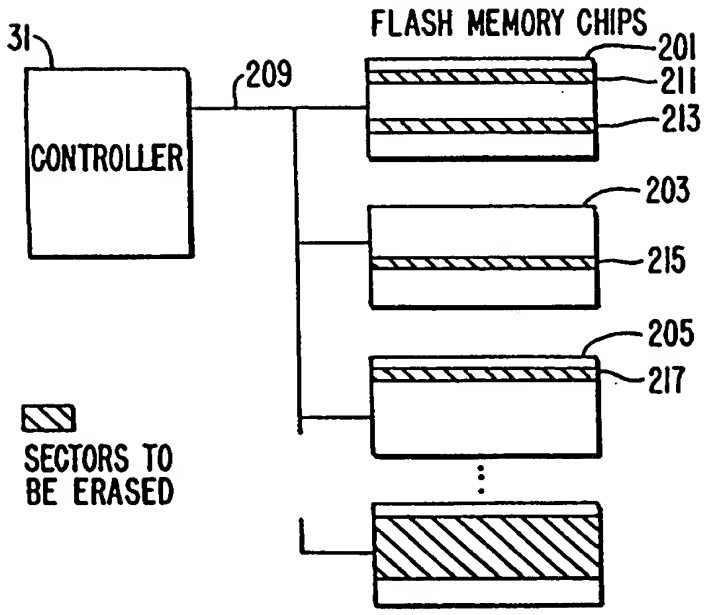

FIG._2

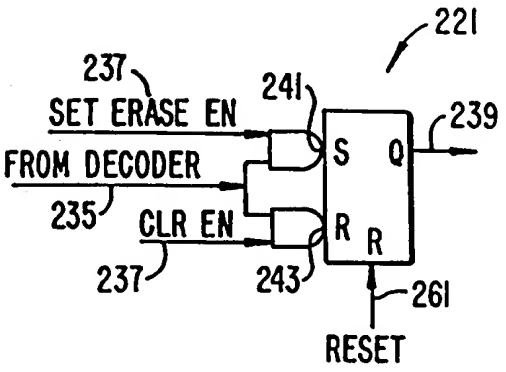

FIG._3B

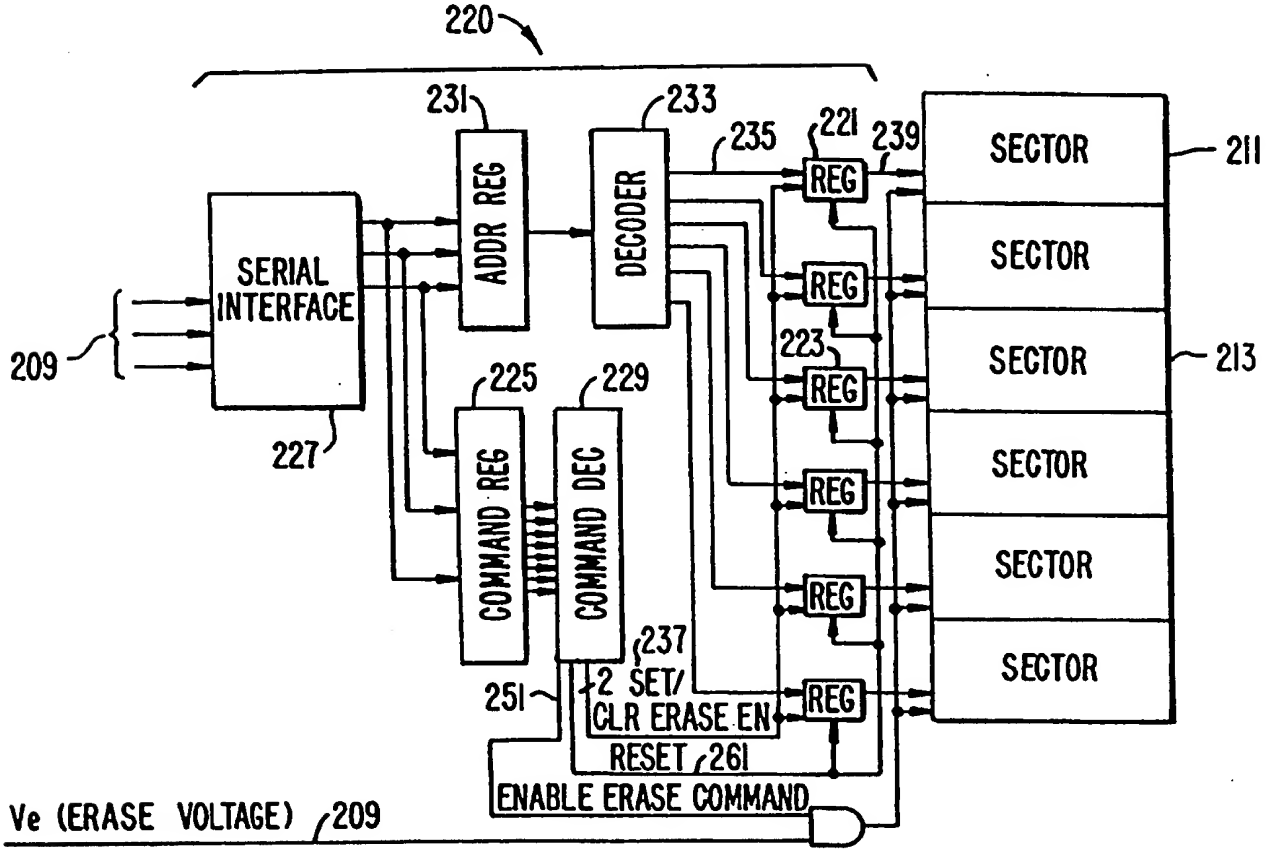

FIG._3A

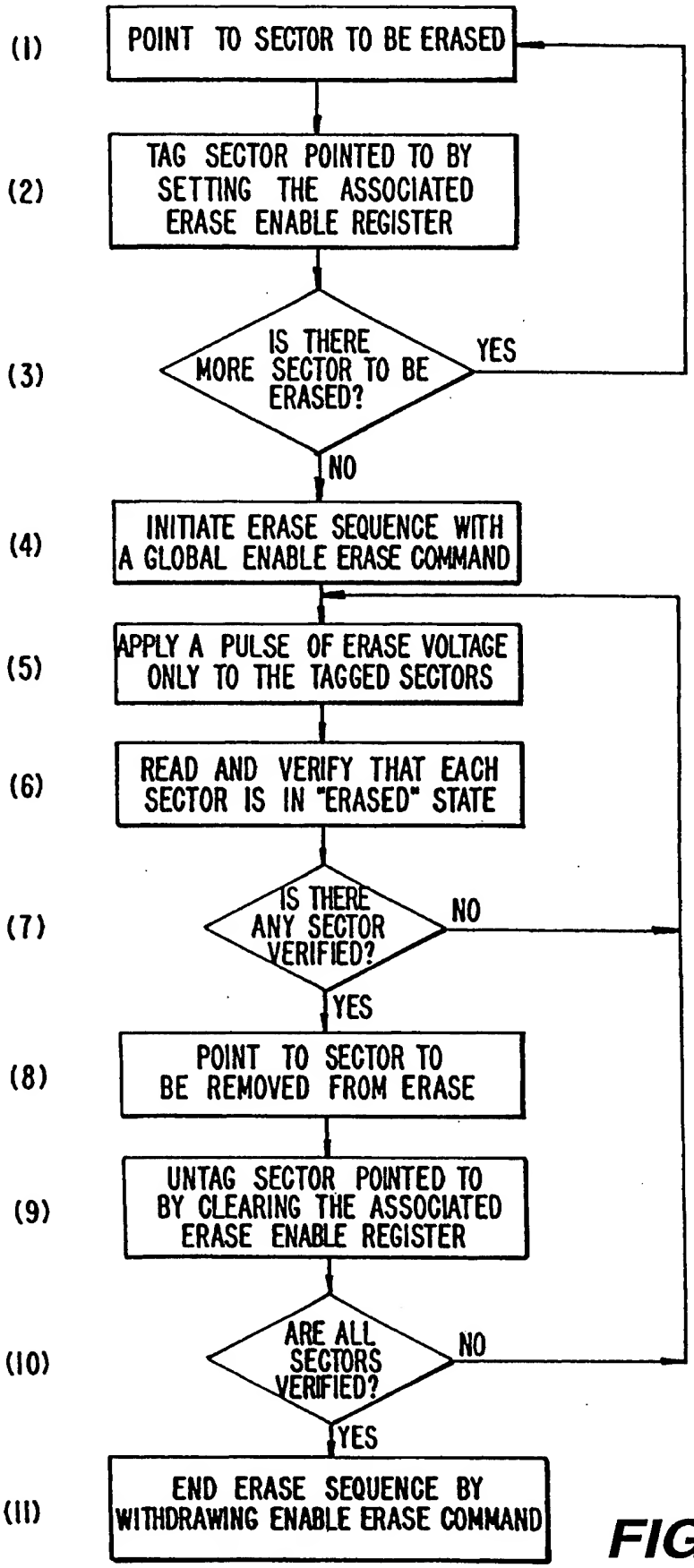

FIG._4

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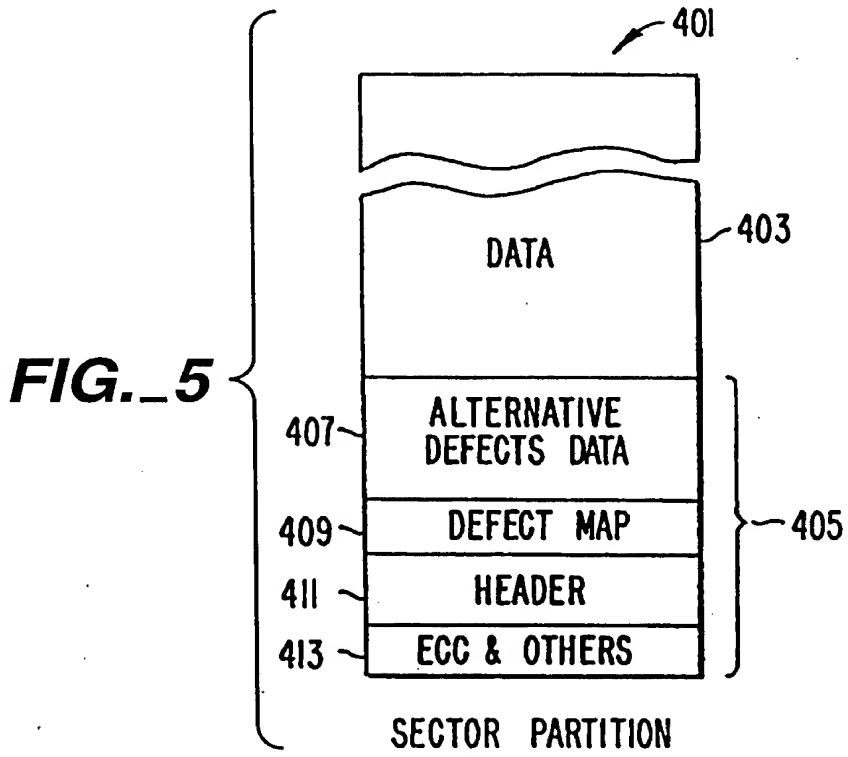

401
DATA
403
ALTERNATIVE DEFECTS DATA
407
DEFECT MAP
409
HEADER
411
ECC & OTHERS
413
405
SECTOR PARTITION

FIG._5

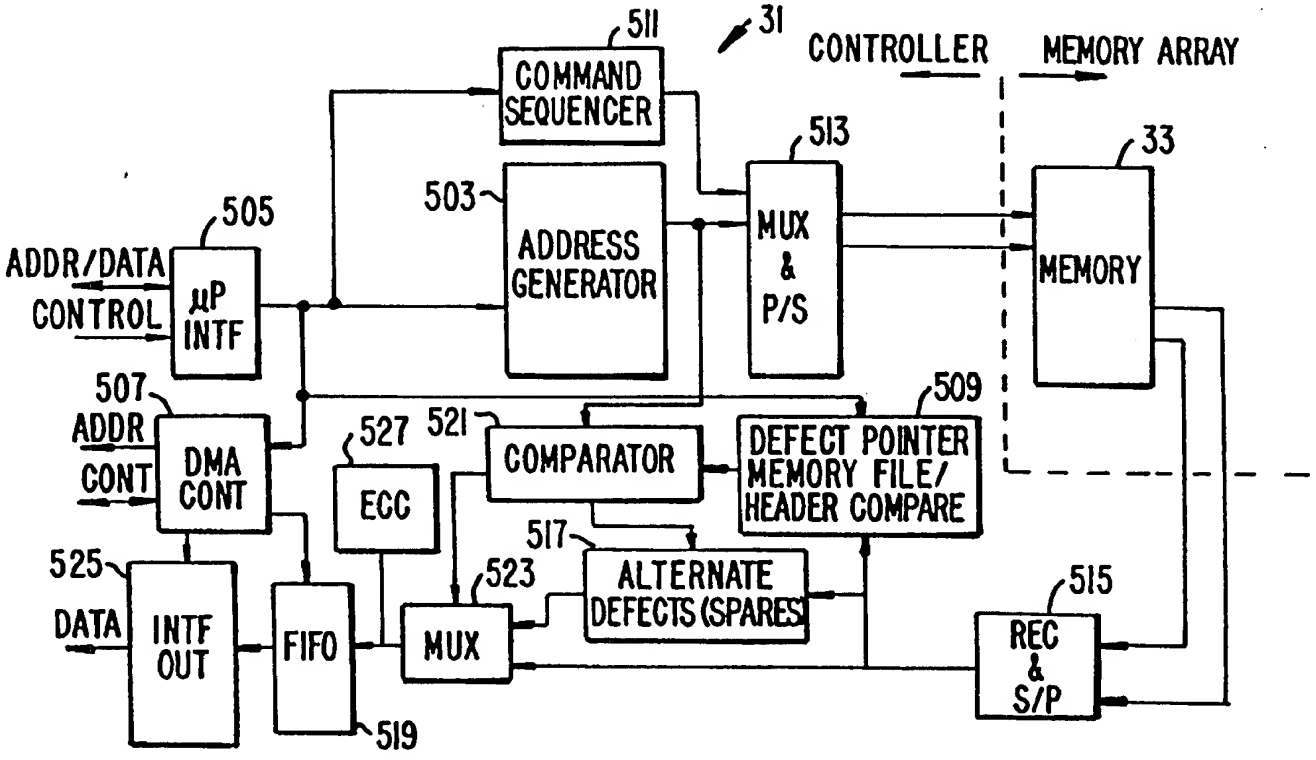
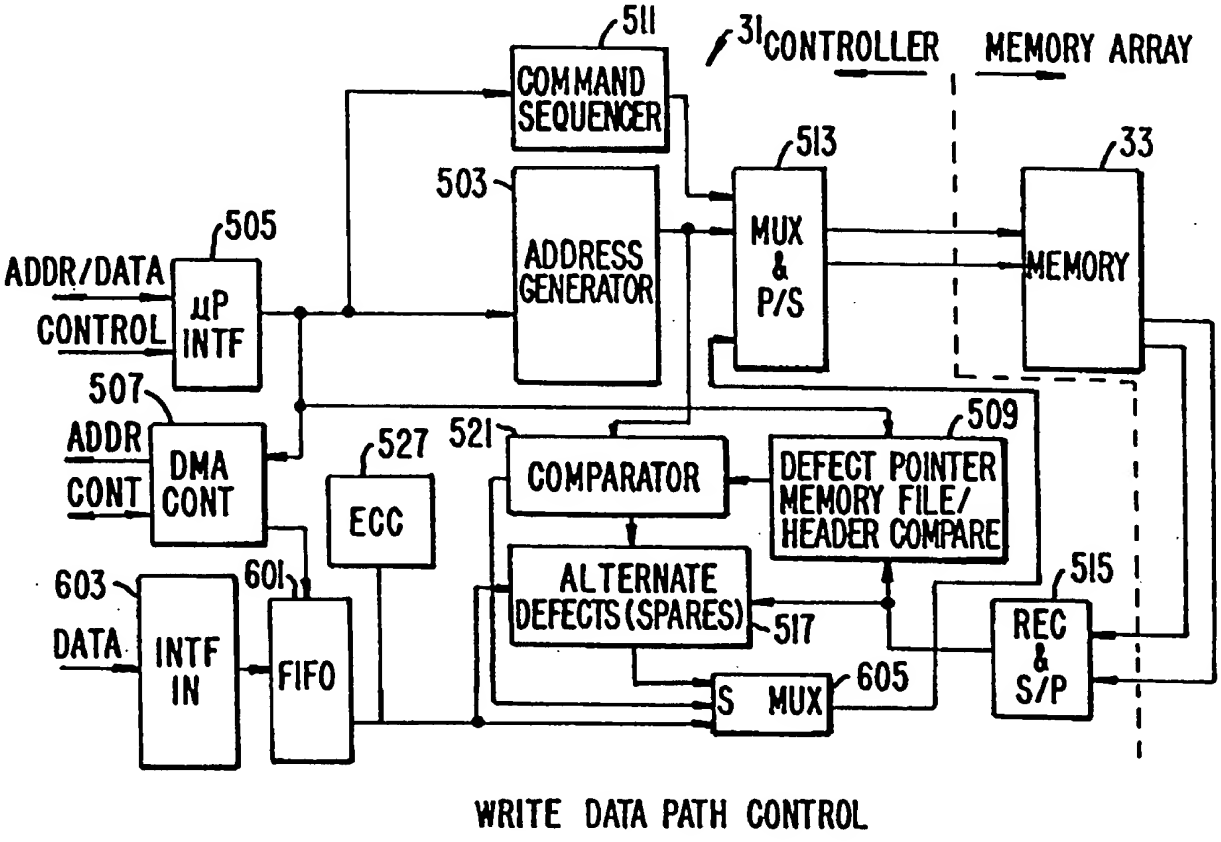

511
31
CONTROLLER
MEMORY ARRAY
COMMAND SEQUENCER
513
33
503
ADDRESS GENERATOR
MUX & P/S
MEMORY
505
ADDR/DATA
CONTROL
μP INTF
507
ADDR
CONT
DMA CONT
527
521
509
COMPARATOR
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
ECC
517
525
523
ALTERNATE DEFECTS (SPARES)
515
DATA
INTF OUT
FIFO
MUX
REC & S/P
519
READ DATA PATH CONTROL

FIG._6



WRITE DATA PATH CONTROL

FIG._7

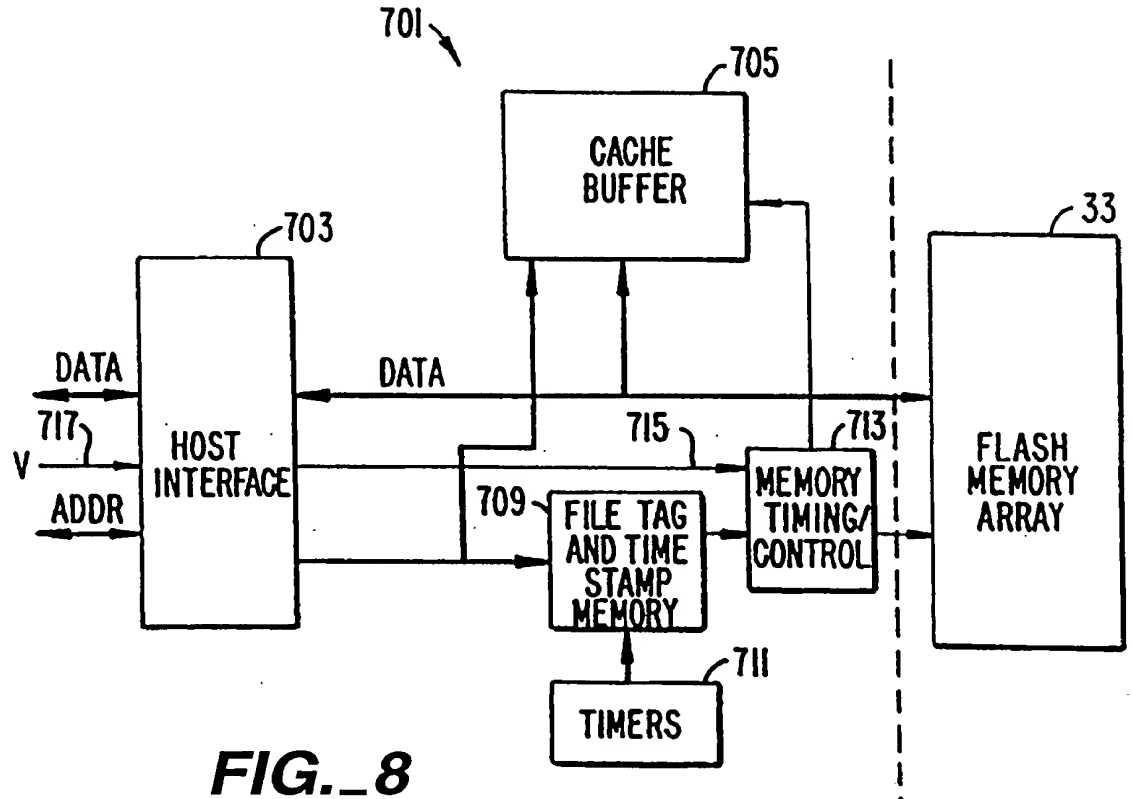


FIG._8

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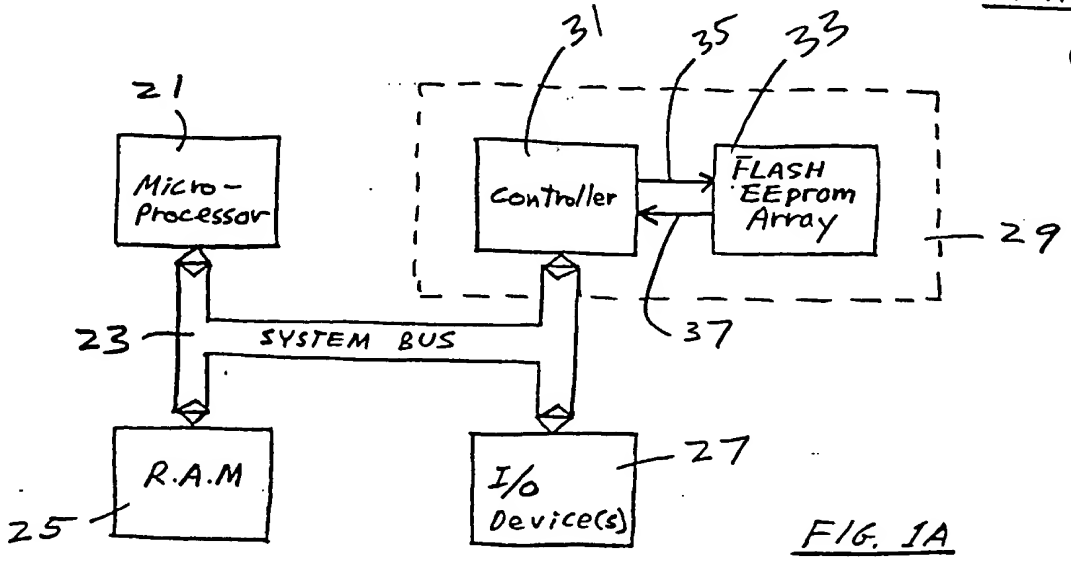


FIG. 1A

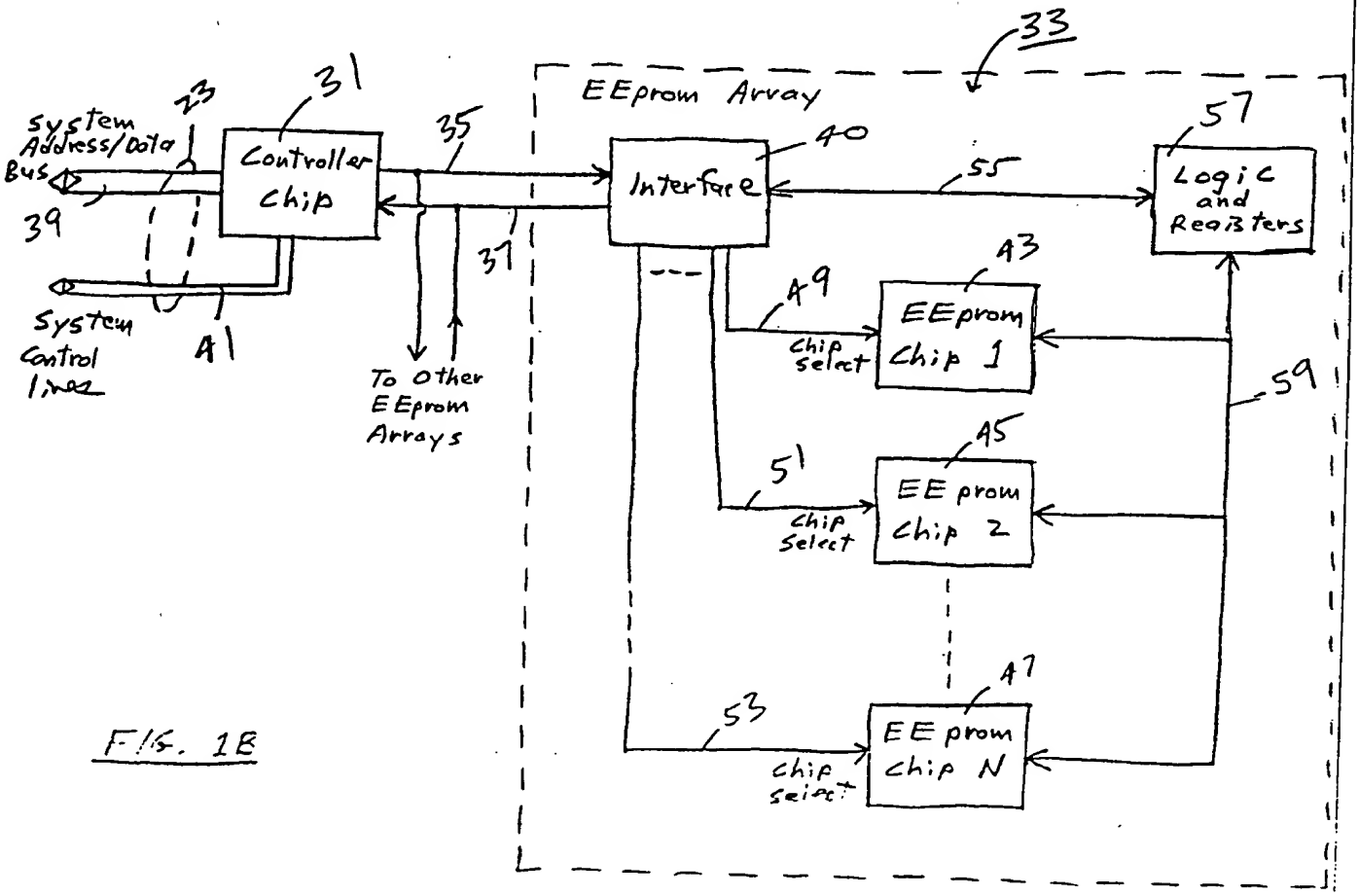


FIG. 1B

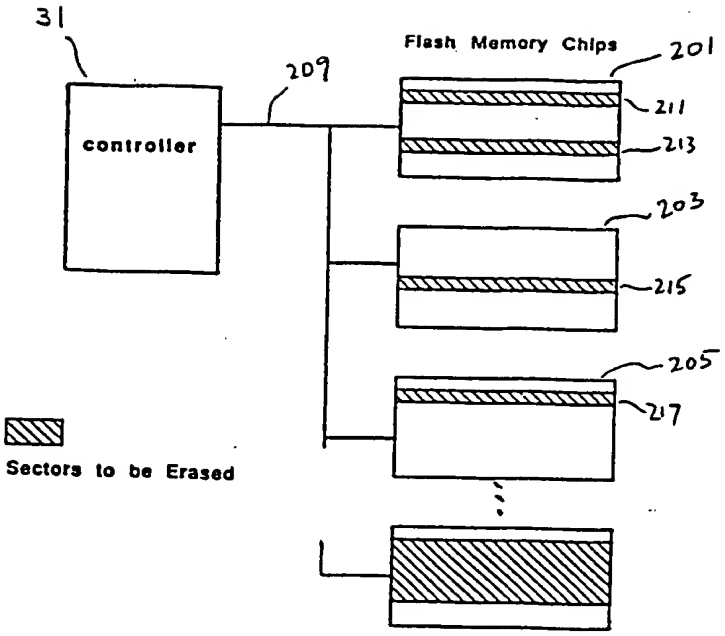


FIG_2

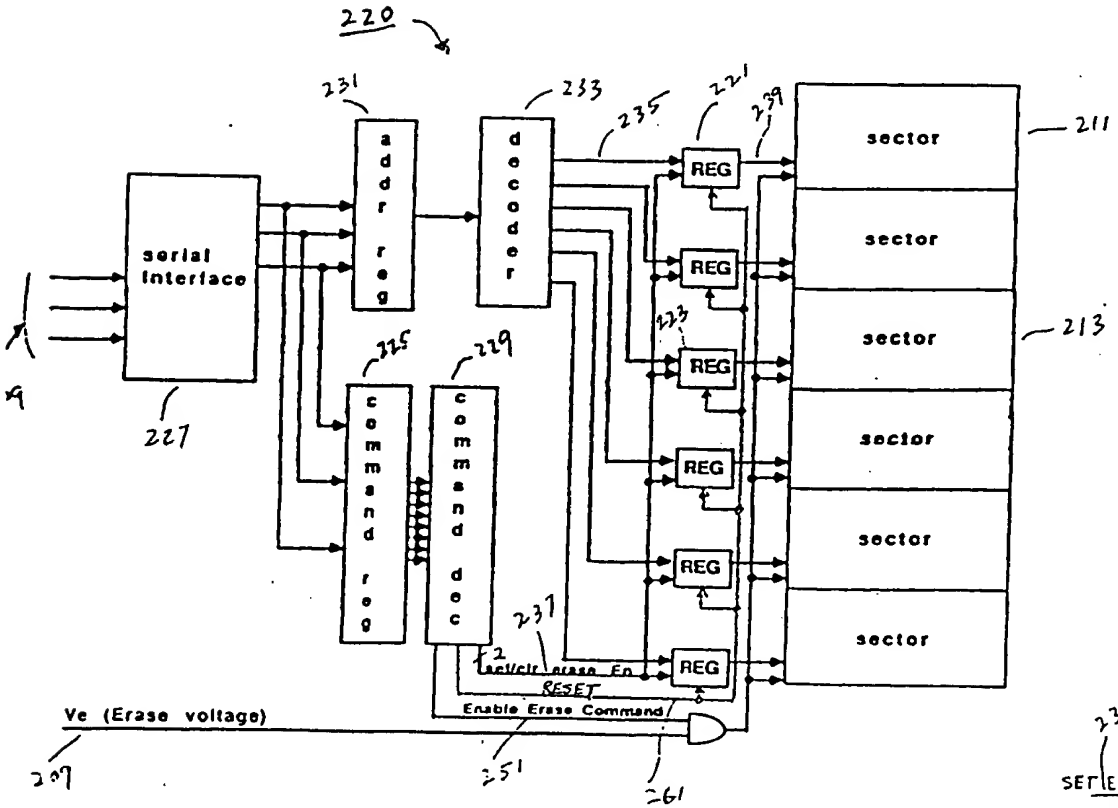


FIG_3A

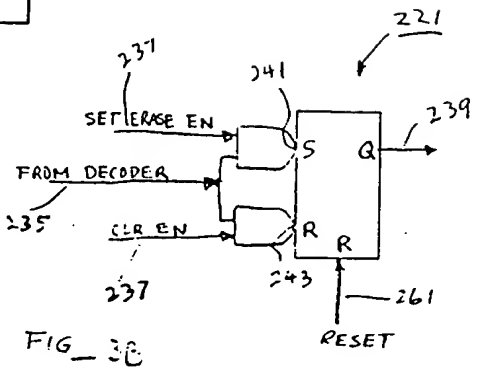


FIG_3B

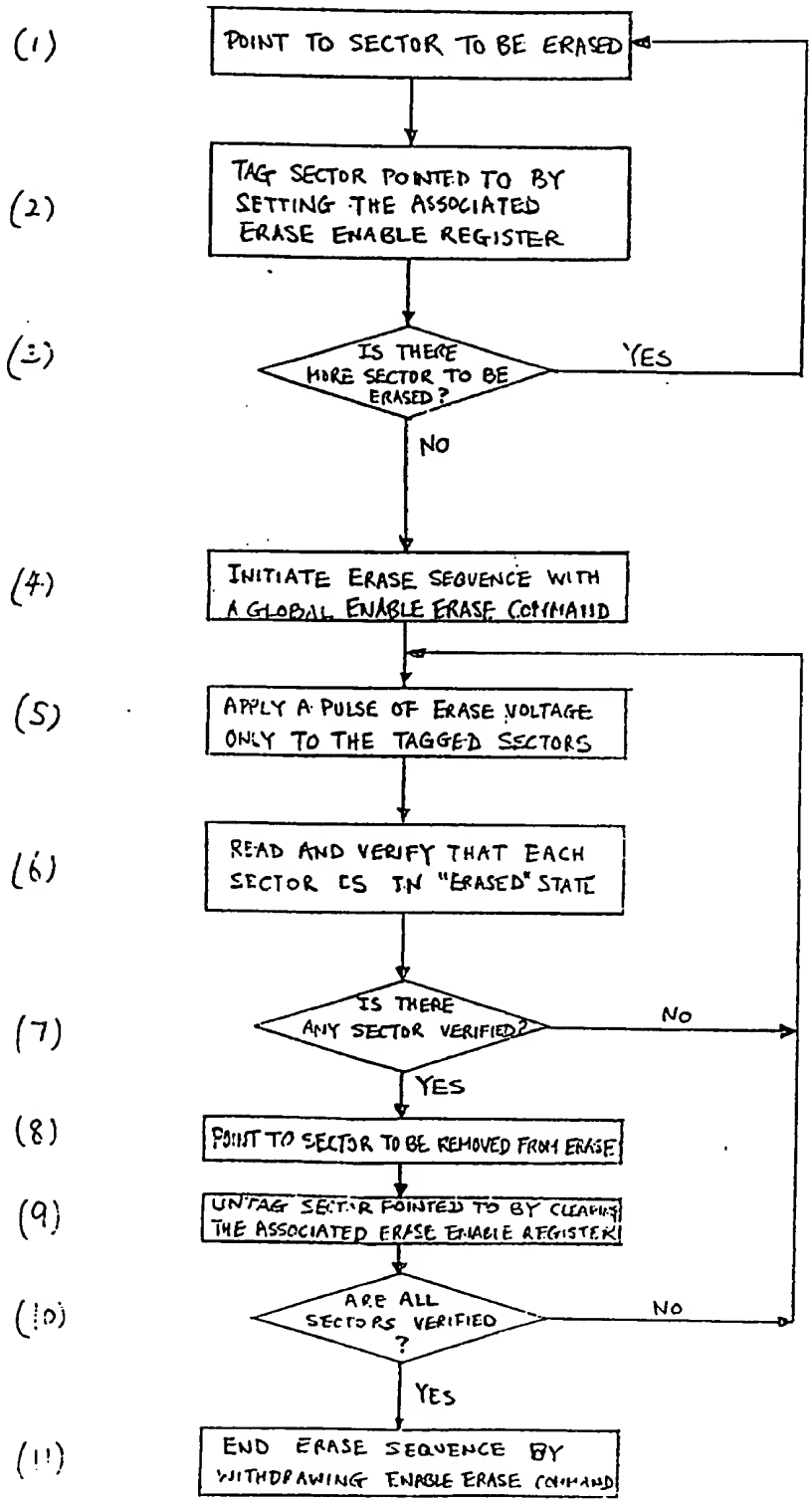
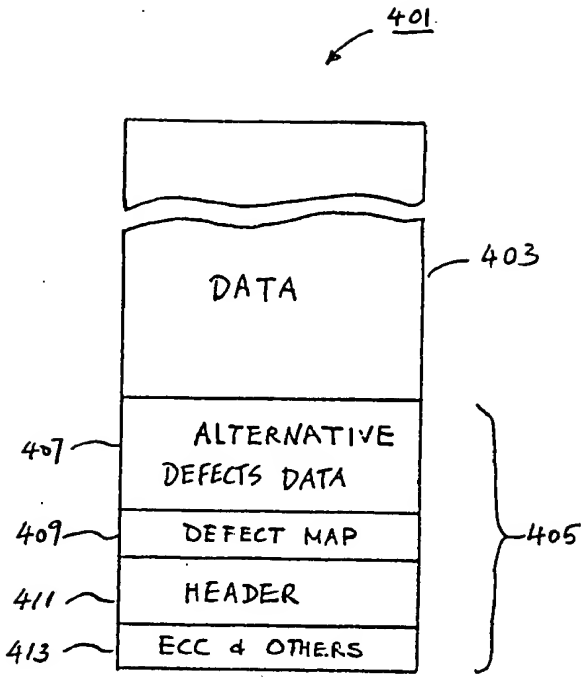
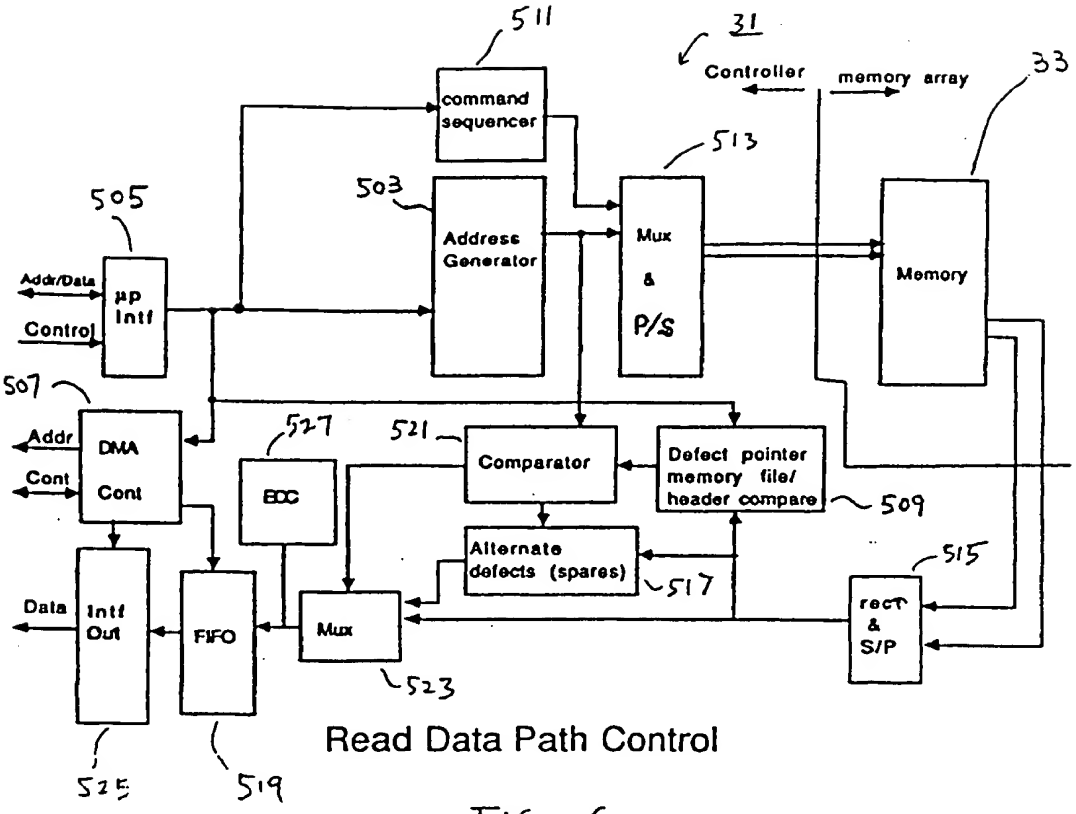

(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
No
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED ?
No
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG_4



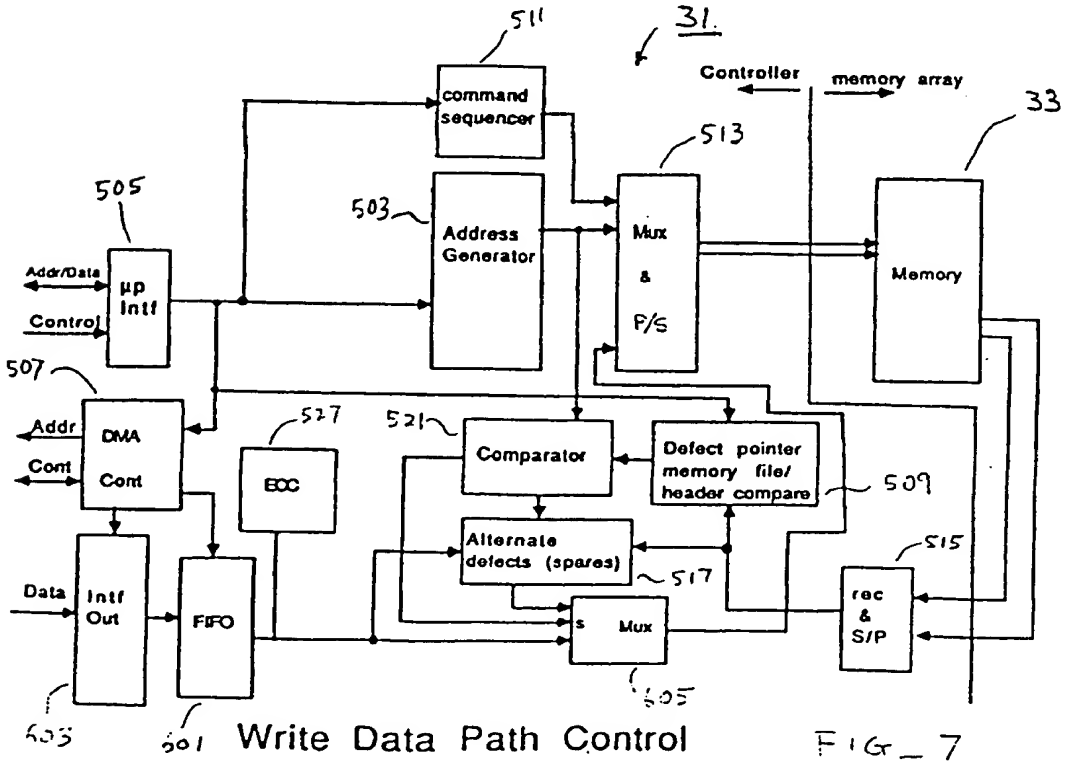
SECTOR PARTITION

FIG_5



Read Data Path Control

FIG_ 6



Write Data Path Control

FIG_ 7

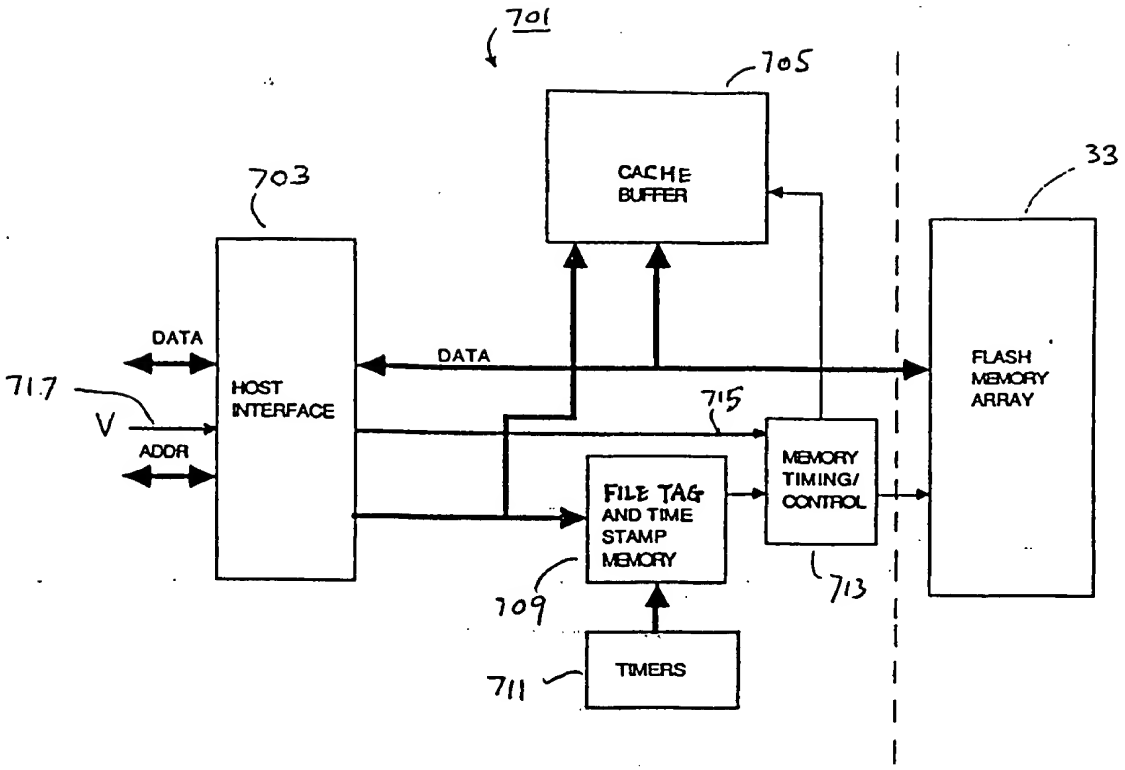

701
705
CACHE BUFFER
703
33
DATA
HOST INTERFACE
DATA
FLASH MEMORY ARRAY
717
V
ADDR
715
MEMORY TIMING/ CONTROL
FILE TAG AND TIME STAMP MEMORY
709
713
TIMERS
711

FIG. 8